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10/531,134	04/13/2005	Adnan Al-Adnani	AAT-102US	5098

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EXAMINER	
SMITH, JOSHUA Y	

ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,134	AL-ADNANI, ADNAN	
	Examiner	Art Unit	
	Joshua Smith	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenbaum et al. (Patent No.: US 6,272,144 B1) in view of Griffin et al. (Patent Number: 5,406,403), hereafter referred to as Berenbaum and Griffin, respectively.

In regards to Claim 1, Berenbaum teaches in column 3, lines 8-12, and in column 4, lines 6-12, and in FIG. 3, Sheet 1 of 3, a line card (item 50, FIG. 3) includes a a transmission convergence (TC) device (item 543, FIG. 3) with an in-band control configuration (Reconfigurable signal processing architecture comprising a reconfigurable data processing module).

Berenbaum also teaches in column 4, lines 12-16, and in column 5, lines 23-27 and 37-44, and in FIG. 4, Sheet 2 of 3, a transmission convergence device interfaces with a Utopia port, which is part of an ATM cell-based switch fabric interconnect with a SONET port, and a message format of a single 53-byte ATM cell (item 70, FIG. 4) for use in transferring control information between a control processor and a transmission convergence device, and a given ATM cell received in a transmission convergence device from a control processor is identified as a control message by the presence of a specific virtual path indicator (VPI)/virtual channel indicator (VCI) address in the ATM header (item 72, FIG. 4) (data is input to a module in a packet frame structure including configuration frames and processing frames, each frame including a header having a mode selection bit indicating whether the frame contains reconfiguration data or processing data, and a module is operable in a reconfiguration mode or a processing mode responsive to a frame header and the mode selection bits are separated from data bits in each frame and are used to control mode selection in the module for determining how incoming data is handled, mode selection bits are separated from data in each frame and are used to control mode selection logic in a module for determining how incoming data is handled).

Berenbaum fails to explicitly teach a module is operable in a reconfiguration mode or a processing mode responsive to a frame header. Griffin teaches these limitations.

In the same field of endeavor, Griffin teaches in column 3, lines 30-43, and in FIG. 3, a DATA I.D. BIT (FIG. 3) in front of and separated from DATA BITS (FIG. 3),

and where a vlau of 1 for the data identification bit may be preselected to indicate a packet contains configuration information, and, is a valid configuration is determined to exist, the transmitter shifts into normal transmit mode (a module is operable in a reconfiguration mode or a processing mode responsive to a frame header). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Griffin with the invention of Berenbaum since Griffin explicitly teaches a transmitter module shifting from a configuration mode to a normal transmit mode, and can be implmented in the apparatus of Berenbaum since it ensures a convergence device of Berenbaum is configured properly prior to further data processing, ensuring that subsequent data is not processed with an incorrect, obsolete, or expired configuration that may result in lost, misused, or misdirected data.

In regards to Claim 2, as discussed in the rejection of Claim 1, Berenbaum teaches a reconfigurable data processing module each of which receives data in a packet frame structure. Berenbaum further teaches a plurality of reconfigurable data processing modules. Berenbaum fails to teach each module is operable in a reconfiguration mode or a processing mode according to a frame header. As discussed in the rejection of Claim 1, Griffin teaches these limitations.

Berenbaum further teaches in column 4, lines 19-24, multiple line cards of an ATM switch (a plurality of reconfigurable data processing modules).

Claims 3-7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenbaum in view of Griffin, and further in view of Laufer et al. ("PCI-PipeRench and the SwordAPI: A System for Stream-based Reconfigurable Computing", 1999, IEEE Comput. Soc., US, p. 303), hereafter referred to as Laufer.

In regards to Claim 3, as discussed in the rejection of Claim 1, Berenbaum teaches a frame header, a mode selection bit, and a module. Bebernbaum fails to teach a bit for each module. Laufer teaches these limitations.

In the same field of endeavor, Laufer teaches in page 203, lower half of first column, a Chip ID tells each chip whether to keep a header or pass it along. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Berenbaum since Laufer provides a technique where a component can determine if it is required to process a packet or pass it to another component, allowing a control processor in the apparatus of Berenbaum to address directly to a component within the apparatus so that components are not required to determine where to forward data within the apparatus through indirect means, such as processing network addresses.

In regards to Claim 4, as discussed in the rejection of Claim 1, Berenbaum teaches mode selection bits, and, as discussed in the rejection of Claim 2, a plurality of modules. Berenbaum further teaches in column 4, lines 37-42, and in FIG. 1, Sheet 1 of 3, an ATM switch fabric, which connects multiple line cards to a control processor in a manner shown in FIG. 1 (a single decoder serving a plurality of modules).

In regards to Claim 5, as discussed in the rejection of Claim 1, Berenbaum teaches that decoded mode selection data is supplied to modules. Berenbaum fails to teach data is supplied in parallel. Griffin further teaches these limitations.

Griffin further teaches in column 4, lines 9-12, rearranging serial data into parallel data (data is supplied in parallel). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Griffin with the invention of Berenbaum since Griffin provides a method of forwarding data in parallel, which can be faster in certain cases than forwarding data in serial.

In regards to Claim 6, as discussed in the rejection of Claim 1, Berenbaum teaches modules. Berenbaum fails to teach modules are connected to each other in series. Laufer teaches these limitations.

In the same field of endeavor, Laufer teaches in page 203, lower half of first column, a number of reconfigurable chips chained together, where the output of each chip is connected directly to the input of the next one (modules are connected to each other in series). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Berenbaum since Laufer provides a system where a convergence device of the apparatus of Berenbaum can be composed of multiple components connected in a chain and that cooperate in processing data so that more data can be processed faster.

In regards to Claims 7 and 11, as discussed in the rejection of Claim 1, Berenbaum teaches modules, incoming data, and a header. Berenbaum fails to teach a bypass mode where data is not acted on by a module and where a header indicates this. Laufer teaches these limitations.

In the same field of endeavor, Laufer teaches in page 203, lower half of the first column to the upper half of the second column, a Chip ID field of a header tells each chip whether to keep the header or pass it along, and when an input controller receives a bare packet, it checks to see if it is currently processing a header, and, if not, the packet must be for a device further on the chain, and the packet is passed on untouched (teach a bypass mode where data is not acted on by a module and where a header indicates this). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Berenbaum since Laufer provides a mode indicated by a header where a component does not act on a packet and simply forwards it to an appropriate component within an apparatus, allowing the apparatus of Berenbaum to deactivate any unnecessary processing of particular packets and speeding up processing whithin the apparatus as a whole.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenbaum in view of Griffin, and further in view of Chieu et al. (Patent No.: US 6,501,807 B1), hereafter referred to as Chieu.

In regards to Claim 8, as discussed in the rejection of Claim 1, Berenbaum teaches digital processing and digital components that are configurable. Berenbaum fails to teach a radio signal processing apparatus where signals are processed digitally. Chieu teaches these limitations.

In the same field of endeavor, Chieu teaches in column 3, lines 45-47, a digital signal processor (DSP) and a radio module (a radio signal processing apparatus where signals are processed digitally). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Chieu with the invention of Berenbaum since Chieu provides an apparatus with components that can allow wireless digital communications, which can be used to extend the apparatus of Berenbaum to include wireless services to customers, such as cellular or WiMAX services.

In regards to Claim 9, as discussed in the rejection of Claim 1, Berenbaum teaches configuration data supplied to a module. Berenbaum fails to teach default data supplied from memory outside a module. Cheiu teaches these limitations.

In the same field of endeavor, Cheiu teaches column 4, lines 46-52, and in FIG. 2, Sheet 1 of 6, a flash memory (item 24, FIG. 2) containing program instructions that are utilized upon initial start-up, where the start-up program is uploaded from the flash memory to a microcontroller (item 22, FIG. 2) and copied to a DRAM (item 23, FIG. 2) (default data supplied from memory outside a module). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of

Chieu with the invention of Berenbaum since Chieu provides a system where a start-up program is stored on non-volatile memory, allowing the apparatus of Berenbaum to reinitialize after being shut down or to recover after a power outage.

In regards to Claim 10, Berenbaum fails to teach a radio signal processing apparatus selected from a group consisting of a receiver, a transmitter, or a transceiver. As discussed in the rejection of Claim 8, Chieu teaches a radio signal processing apparatus. Chieu further teaches a receiver and a transmitter. Chieu further teaches in column 2, line 66 to column 4, line 6, and in FIG. 1, Sheet 1 of 6, a transmitter portion, a receiver portion, and a hybrid (a group consisting of a receiver, a transmitter, or a transceiver). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Chieu with the invention of Berenbaum since Chieu provides an apparatus with components that can allow wireless digital communications, which can be used to extend the apparatus of Berenbaum to include wireless services to customers, such as cellular or WiMAX services.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Smith whose telephone number is 571-270-1826. The examiner can normally be reached on Monday through Friday, 9:30 AM to 7:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joshua Smith
12/17/2007

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SUPERVISORY PATENT EXAMINER